

What is claimed is:

1. An A/D converter, comprising:

a plurality of capacitors and at least one comparator,

arranged to form an analog to digital conversion of an analog

input signal to a digital output signal; and

a control circuit, controlling said capacitors to be used

for both analog to digital conversion and for calibration.

2. A converter as in claim 1, wherein said control circuit

controls a level which is supplied to said capacitors.

3. A converter as in claim 1, further comprising a

plurality of level latches, storing levels associated with

calibration, and connected to control respective levels applied

to said capacitors.

4. A converter as in claim 2, wherein said control circuit

controls a level which is supplied to a bottom plate of each

said capacitor, and wherein a top plate of each said capacitor

is connected together to form a common line.

5. A converter as in claim 2, further comprising an image

acquisition element, obtaining information indicative of a

3 portion of an image, and producing an output indicative thereof,
 4 said an output being analog to digitally converted by said
 5 analog to digital converter.

1 6. A converter as in claim 4, wherein said level supplied
 2 to a bottom plate of each said capacitors can be one of two
 3 different voltage levels or a ground level.

1 7. A converter as in claim 4, wherein said level applied
 2 to a bottom plate of each capacitor can be a first voltage level
 3 which is double a value of said first voltage level.

1 (8.) A converter as in claim 5, wherein said image
 2 acquisition element is a MOS element.

1 (9.) A converter as in claim 8, wherein said image
 2 acquisition element is one of a MOS photo diode or a MOS photo
 3 gate, and forms an active pixel sensor.

1 10. A converter as in claim 1, wherein said control
 2 circuit includes a latch, latching a level which is supplied to
 3 a bottom plate of each of a plurality of capacitors.

1 11. A converter as in claim 10, wherein said level can be
2 one of ground or one of two voltage levels.

1 12. A converter as in claim 10, wherein said level can be
2 one of ground or a single voltage level.

1 13. A converter as in claim 12, further comprising a
2 plurality of level latches, respectively storing levels
3 associated with calibration, and connected to control a level
4 applied to said capacitors.

1 14. A converter as in claim 13, wherein said level latches
2 store a negative version of a calibration level.

1 15. A converter as in claim 14, wherein said negative
2 version is a two's compliment.

1 16. An A/D converter comprising:
2 a plurality of capacitors, each associated with a specified
3 bit of the digital signal, and each having a top plate connected
4 to a common line and a bottom plate, and a comparator, connected
5 to receive said common line as an output of said capacitor at
6 one input, and a signal at another input; and

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7 a plurality of value latches, each storing a value, and
 8 each associated with one of said plurality of capacitors, and
 9 changing a value applied to said bottom plate of said capacitor.

1 17. A converter as in claim 16, wherein said latches store
 2 either a one or a zero, and apply either a ground level or a
 3 reference level to said capacitor bottom plates depending on the
 4 value stored by said latches.

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 1 18. A converter as in claim 16, further comprising a
 2 control circuit, controlling said value latches to store a
 3 calibration value, and use said calibration value during
 4 converting.

1 19. A converter as in claim 18, wherein the same said
 2 capacitors are used both for calibration and for A/D conversion.

1 20. A converter as in claim 17, wherein said reference
 2 level includes two reference levels, one higher than the other.

1 21. A converter as in claim 17, wherein said reference
 2 level includes a single reference level.

22. A converter as in claim 17, further comprising a switch, controlled by a level in said latch, and selectively providing either a ground level or a reference level to said capacitor.

23. A converter as in claim 18, further comprising an image sensing element, producing an output signal indicative of a portion of said image, said output signal being coupled to said plurality of capacitors and comparator to be A/D converted thereby.

24. A converter as in claim 23, wherein said image sensing element is an element formed in MOS.

25. A converter as in claim 23, wherein said image sensing element is an active pixel sensor, having a photoreceptor, a follower associated with said photoreceptor, and a selector which allows electronic selection, also associated with said photoreceptor.

26. A converter as in claim 25, wherein said image sensing element is one of a photo diode or a photo gate.

27. A converter as in claim 25, wherein said follower and said selector are each formed using CMOS.

28. A converter as in claim 27, wherein said value latches are each formed using CMOS.

29. A converter as in claim 28, wherein said value latches, said comparator and said capacitors, and a plurality of said image sensing elements, are each formed on a common substrate.

30. A converter as in claim 18, wherein said value latches are formed of CMOS.

31. A converter as in claim 18, wherein said value latches store a value calibration value.

32. A converter as in claim 18, wherein said value latches store a negative of a calibration value.

33. A method, comprising:
calibrating an A/D converter using first capacitors;
obtaining a signal to be converted by said A/D converter;
and

5 converting said signal to digital using at least a
6 plurality of said first capacitors for said converting.

1 34. A method as in claim 33, further comprising obtaining
2 values associated with said calibrating, and storing said values
3 in a memory.

1 35. A method as in claim 34, wherein said memory includes
2 a plurality of bits associated with said capacitors, each bit
3 storing a value which adjusts a level that is applied to each
4 said capacitor.

1 36. A method as in claim 35, wherein said level is applied
2 to a bottom plate of said capacitor, and a conversion is carried
3 out using a top plate of said capacitor.

1 37. A method as in claim 33, further comprising applying a
2 calibration level to at least one of said capacitors.

1 38. A method as in claim 33, further comprising storing a
2 calibration level obtained during said calibrating, and using
3 the stored calibration level to apply a calibration level to at
4 least one of said capacitors based on a level of said
5 calibration.

39. A method as in claim 38, wherein said level includes a single reference level and a ground level.

40. A method as in claim 38, wherein said level includes two different reference levels and a ground level.

41. A method as in claim 33, further comprising obtaining a signal indicative of a portion of an image, and using said signal for said converting.

42. A method as in claim 41, wherein said obtaining a signal comprises attaining a signal on the same substrate as said A/D converter.

43. A method as in claim 34, wherein said values include values directly obtained from said calibrating.

44. A method as in claim 34, wherein said values include complements of values obtained during said calibrating.

45. A method as in claim 33, wherein said calibrating further comprising obtaining a complement of a calibration level and storing said complement in a plurality of latch elements.

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1 46. A method as in claim 33, further comprising storing a
2 level associated with said calibrating in a plurality of latch
3 elements, associating each of said latch elements with one of
4 said first capacitors, and using said values to adjust a level
5 on said capacitors according to a calibration level, during
6 obtaining a signal.

1 47. A method, comprising:
2 obtaining a value indicative of calibration of an A/D
3 converter using a plurality of capacitors to obtain said value;
4 storing said value in a latch associated with the A/D
5 converter; and
6 converting an input value using said plurality of
7 capacitors, and using said value stored in said latch.

1 48. A method as in claim 47, wherein said value stored in
2 said latch is a multiple bit value, and associating its of said
3 value stored in the latch with individual ones of said plurality
4 of capacitors.

1 49. A method as in claim 48, further comprising using said
2 value stored in said us a value of said capacitor.

1 50. A method as in claim 48, further comprising using said
2 value to adjust a level applied to a bottom plate of said
3 capacitor.

1 51. A method as in claim 47, wherein said input value is a
2 value indicative of a portion of an image.

1 52. An active pixel sensor, comprising:
2 a semiconductor substrate, having a plurality of items
3 formed thereon, said items including:

4 an image acquisition element, formed using MOS formation
5 technology, and having an MOS follower associated therewith and
6 an MOS selection transistor associated therewith, said image
7 acquisition element producing an output signal indicative
8 thereof; and

9 an A/D converter element, also formed using MOS formation
10 technology, including a plurality of capacitors and a
11 comparator, said plurality of capacitors operating both to
12 calibrate said A/D converter element and to convert signals
13 applied to said A/D converter element, the same capacitors being
14 used both for said calibrate and for said converter, and further
15 comprising a latch, having a plurality of digital storage
16 portions, each formed of CMOS, and each storing a value based on

17 said calibrate, said values used for allowing said A/D converter
18 to acquire signals.

1 53. A sensor as in claim 52, wherein said A/D converter is
2 a successive approximation A/D converter.

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